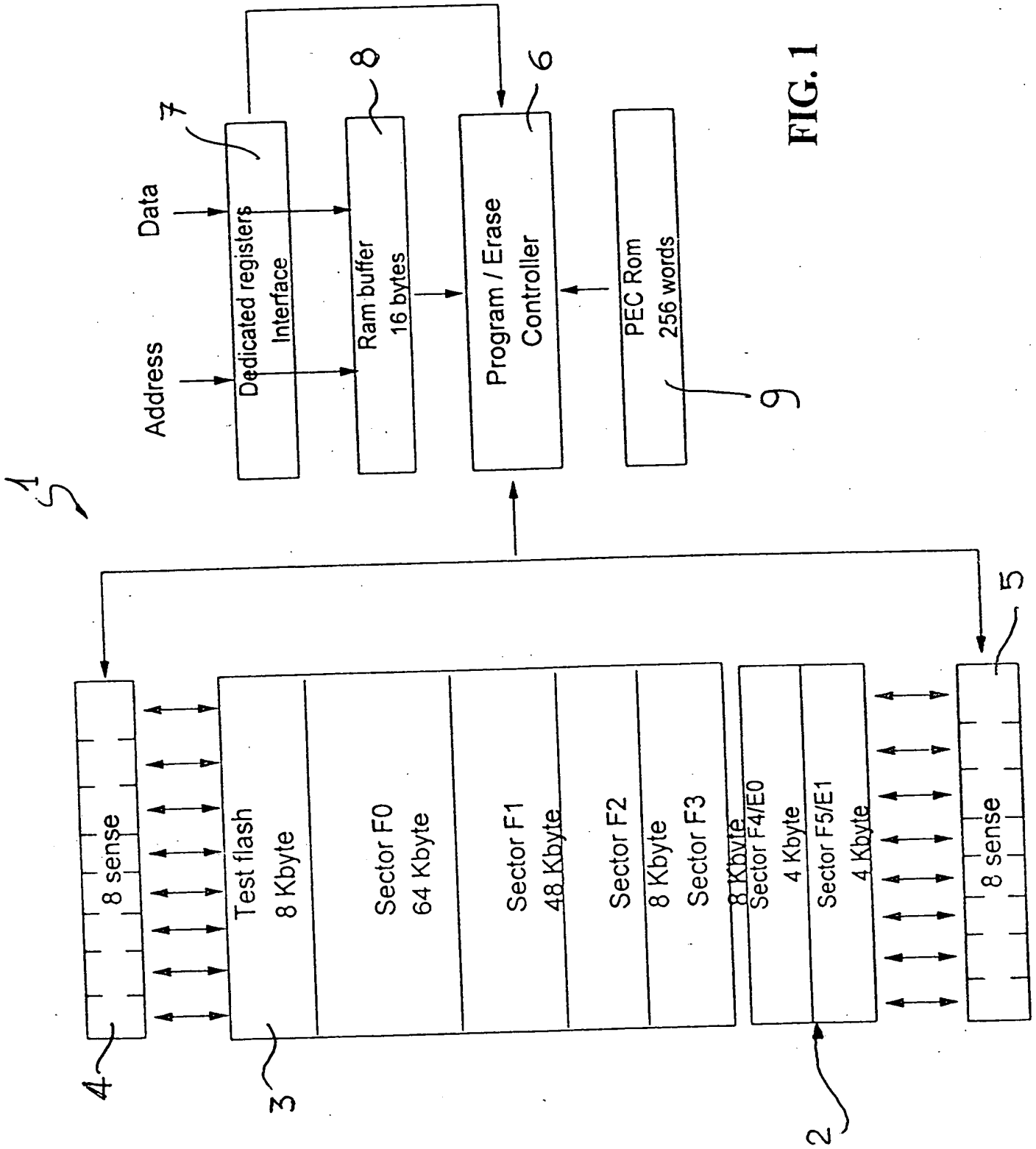
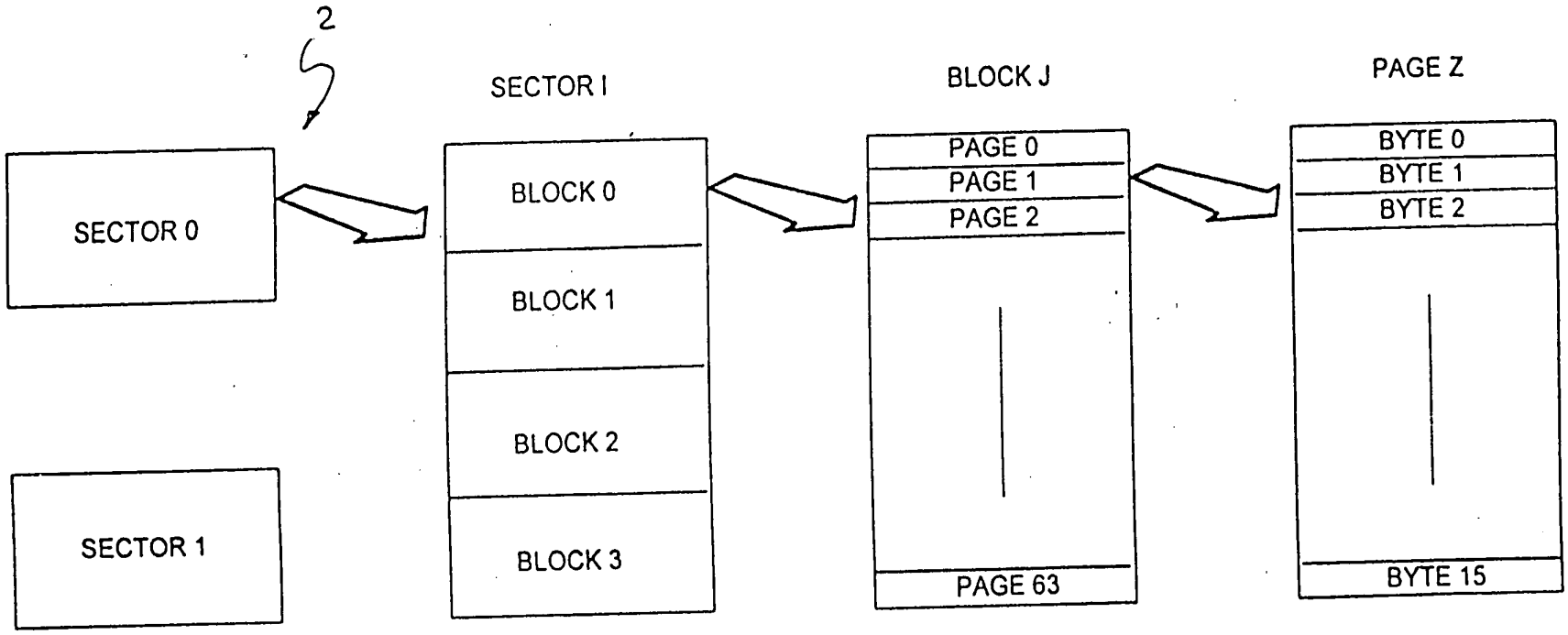

1
Address
Data
Dedicated registers Interface
7
Ram buffer 16 bytes
8
Program / Erase Controller
6
PEC Rom 256 words
9
8 sense
4
Test flash 8 Kbyte
Sector F0 64 Kbyte
Sector F1 48 Kbyte
Sector F2 8 Kbyte
Sector F3 8 Kbyte
3
Sector F4/E0 4 Kbyte
Sector F5/E1 4 Kbyte
2
8 sense
5

FIG. 1



SECTOR: Minimal Erasable Area

BLOCK: Emulated EEprom Address Space

PAGE: Minimal EEprom Update Area

FIG. 2

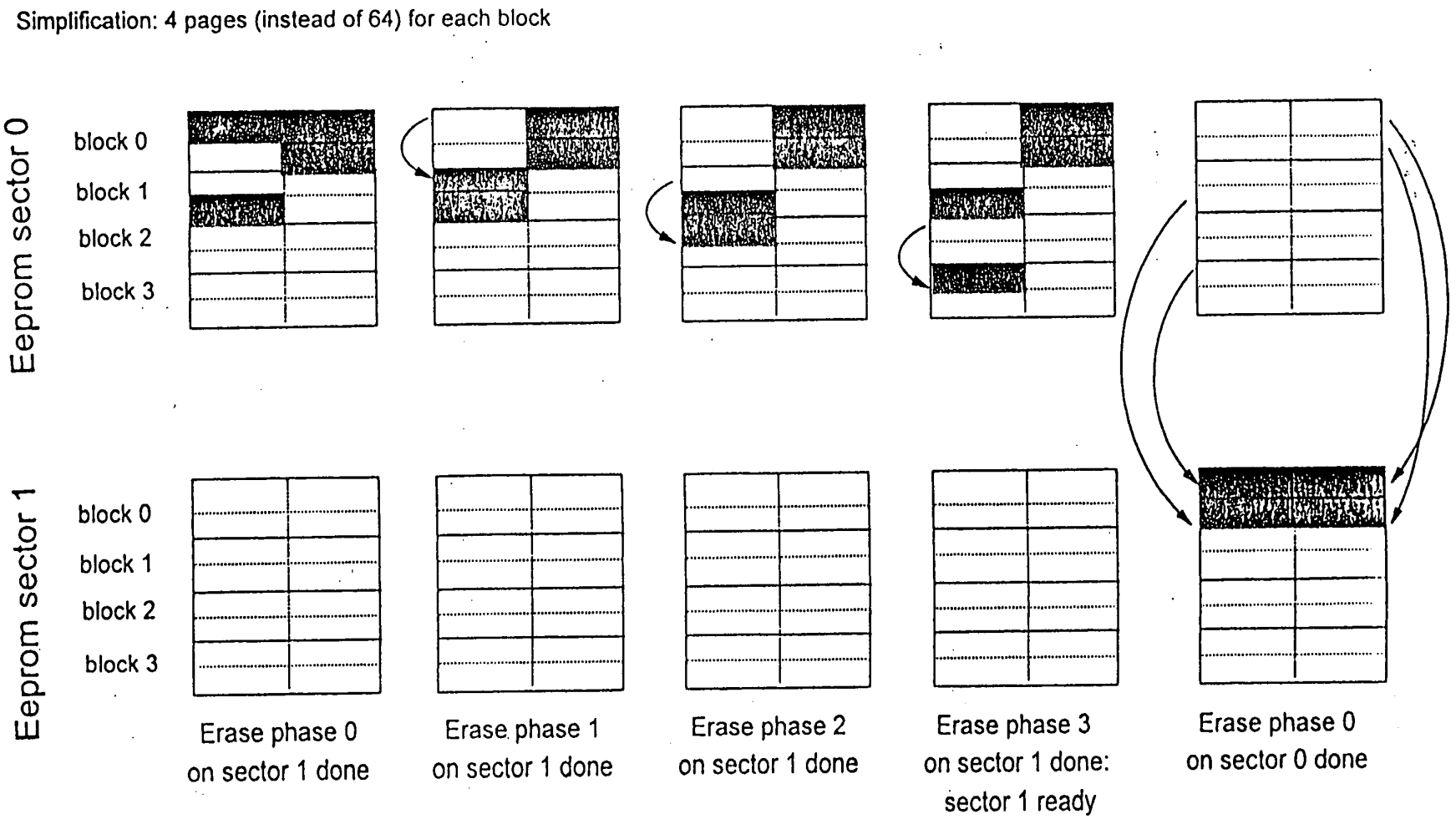

Simplification: 4 pages (instead of 64) for each block
Eeprom sector 0
block 0
block 1
block 2
block 3
Eeprom sector 1
block 0
block 1
block 2
block 3
Erase phase 0 on sector 1 done
Erase phase 1 on sector 1 done
Erase phase 2 on sector 1 done
Erase phase 3 on sector 1 done: sector 1 ready
Erase phase 0 on sector 0 done

FIG. 3

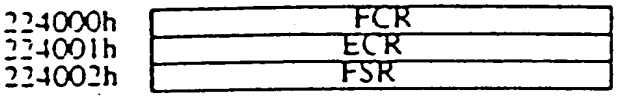


FIG. 3A

Sector	Addresses	Max Size
OTP	211F80h to 211FFFh	128 byte
Flash 0	000000h to 00FFFFh	64 Kbyte
Flash 1	010000h to 01BFFFh	48 Kbyte
Flash 2	01C000h to 01DFFFh	8 Kbyte
Flash 3	01E000h to 01FFFFh	8 Kbyte
Eeprom	220000h to 2203FFh	1 Kbyte

FIG. 3B

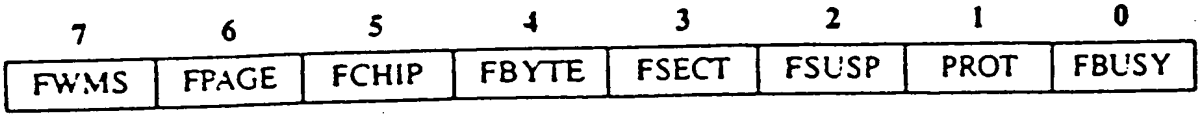


FIG. 3C

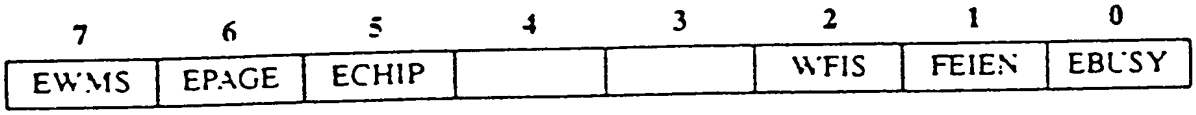


FIG. 3D

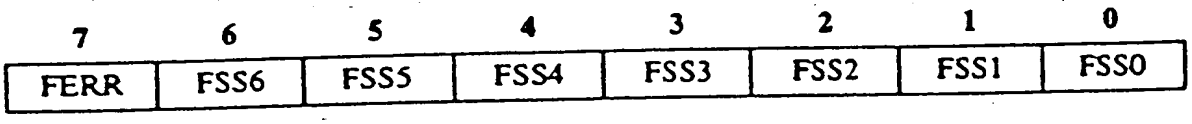


FIG. 3E

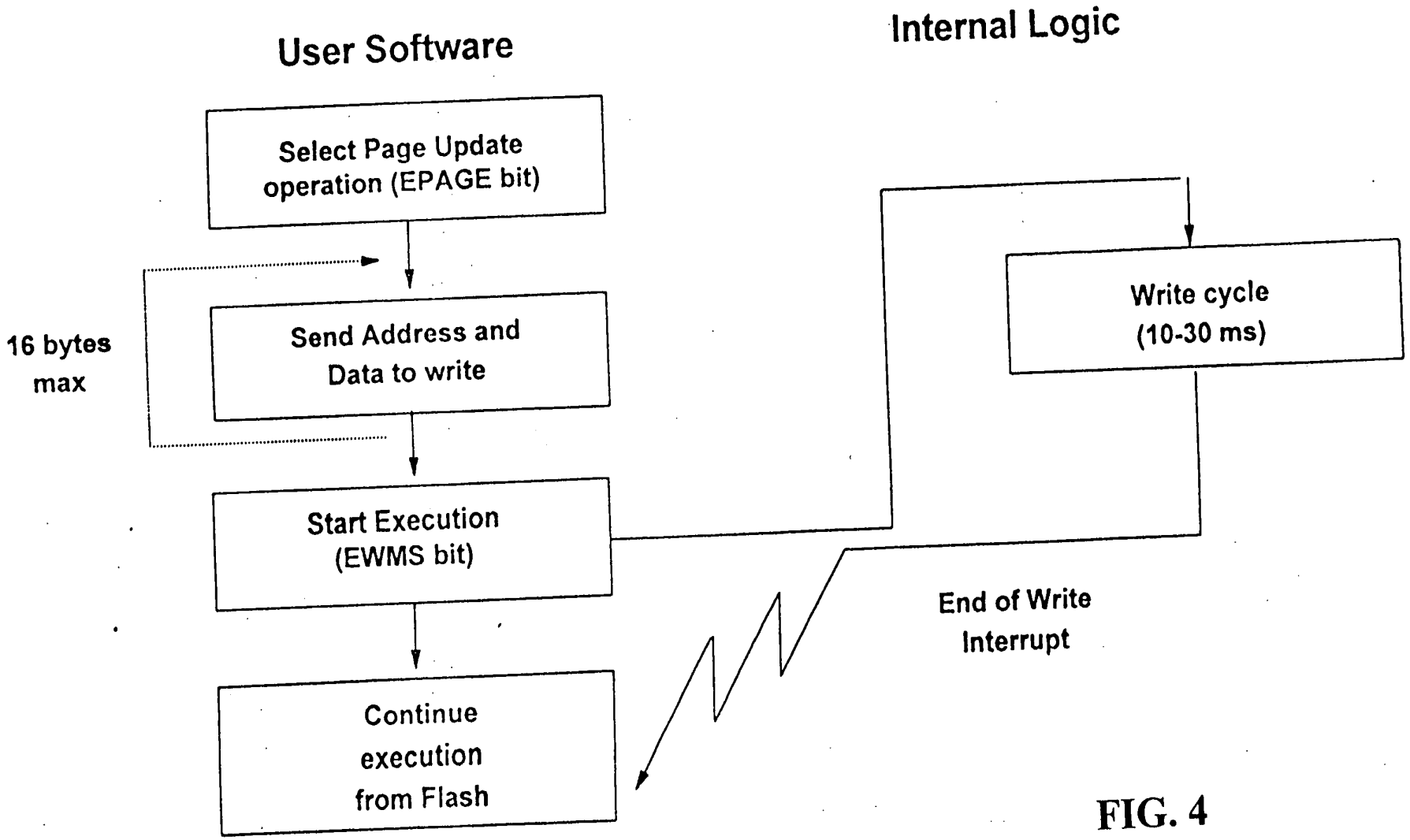

User Software
Internal Logic
Select Page Update operation (EPAGE bit)
Send Address and Data to write
16 bytes max
Start Execution (EWMS bit)
Continue execution from Flash
Write cycle (10-30 ms)
End of Write Interrupt

FIG. 4

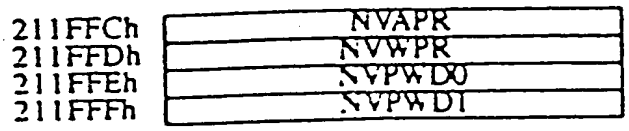


FIG. 4A

Operation	Size	Min	Typ	Max
Page Update	256 byte	160 us	10 ms	30 ms
	512 byte	160 us	15 ms	50 ms
	1 Kbyte	160 us	30 ms	100 ms
Chip Erase	256 byte		35 ms	100 ms
	512 byte		45 ms	150 ms
	1 Kbyte		70 ms	300 ms

FIG. 4B

7	6	5	4	3	2	1	0
APRA	APRO	APBR	APEE	APEX	PWT2	PWT1	PWT0

FIG. 4C

7	6	5	4	3	2	1	0
TMDIS	PWOK	WPBR	WPEE	WPRS3	WPRS2	WPRS1	WPRS0

FIG. 4D

7	6	5	4	3	2	1	0
PWD7	PWD6	PWD5	PWD4	PWD3	PWD2	PWD1	PWD0

FIG. 4E

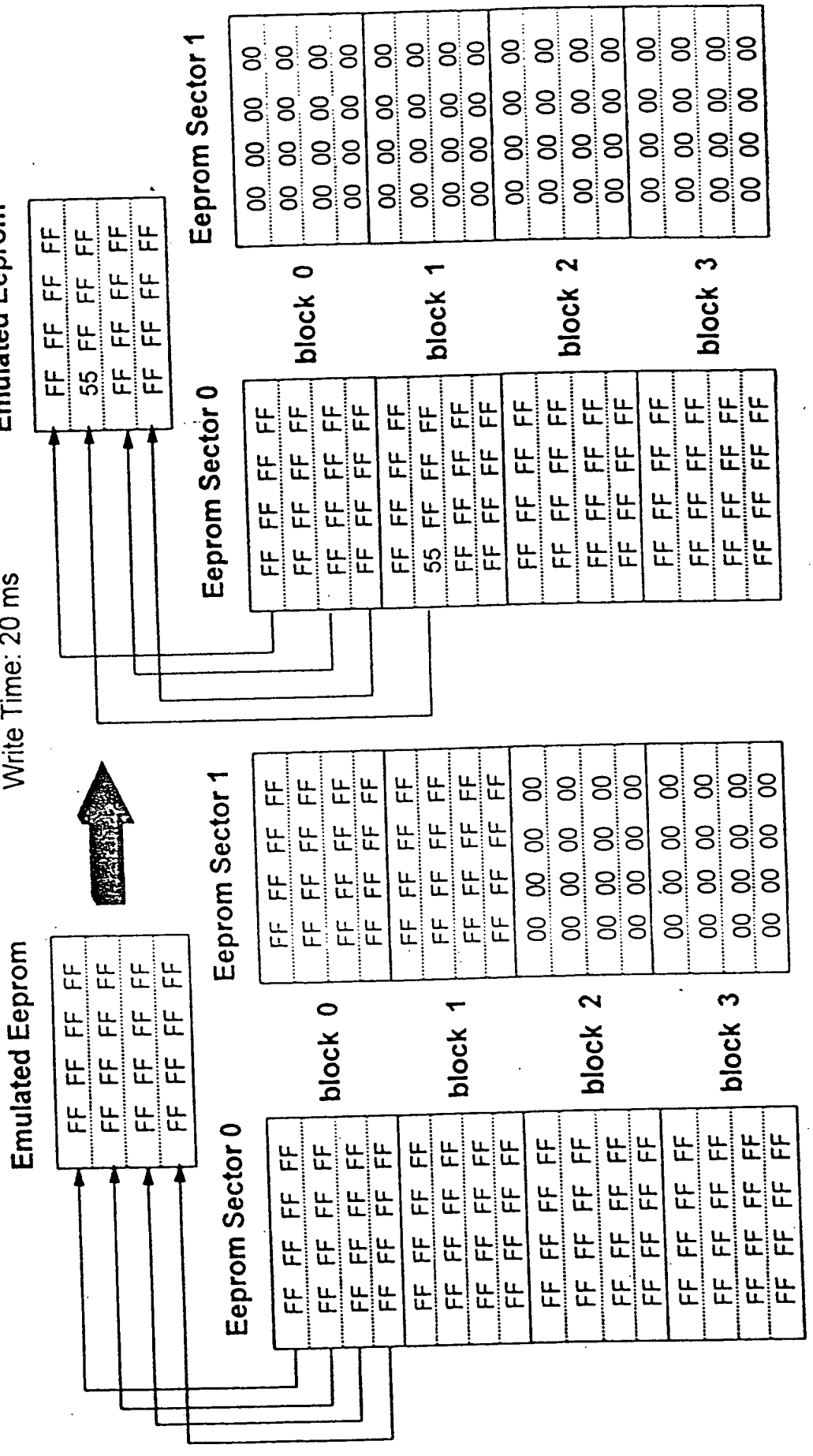

Emulated Eeprom
FF FF FF FF
FF FF FF FF
55 FF FF FF
FF FF FF FF
FF FF FF FF
Eeprom Sector 1
Eeprom Sector 0
block 0
block 1
block 2
block 3
Write Time: 20 ms
Emulated Eeprom
FF FF FF FF
FF FF FF FF
FF FF FF FF
FF FF FF FF
FF FF FF FF
Eeprom Sector 1
Eeprom Sector 0
block 0
block 1
block 2
block 3

FIG. 5

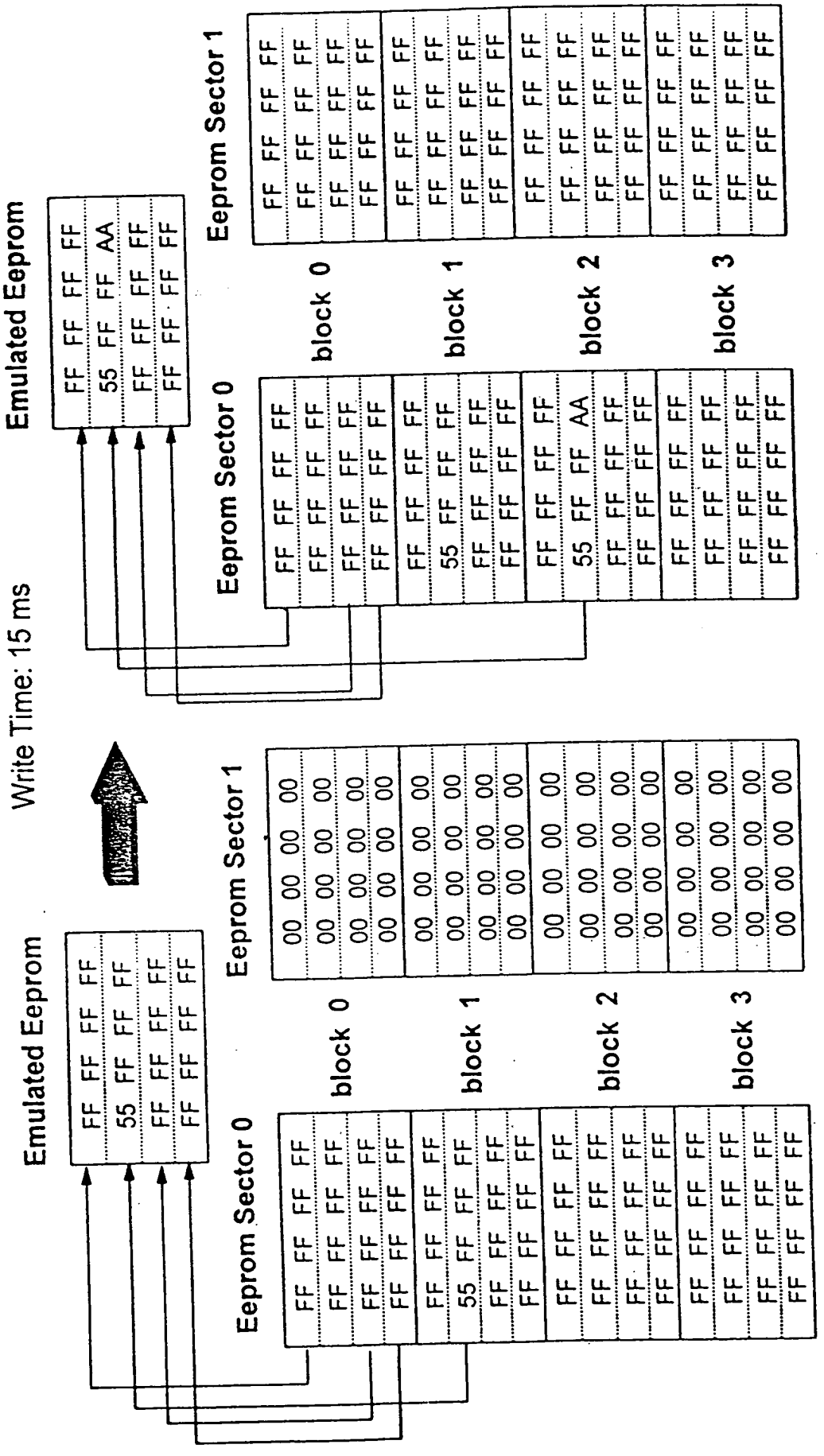

Emulated Eeprom
FF FF FF FF FF
55 FF FF FF FF
FF FF FF FF FF
FF FF FF FF FF
Eeprom Sector 0
Eeprom Sector 1
block 0
block 1
block 2
block 3
Write Time: 15 ms
Emulated Eeprom
FF FF FF FF FF
55 FF FF FF FF
FF FF FF FF FF
FF FF FF FF FF
Eeprom Sector 0
Eeprom Sector 1
block 0
block 1
block 2
block 3

FIG. 6

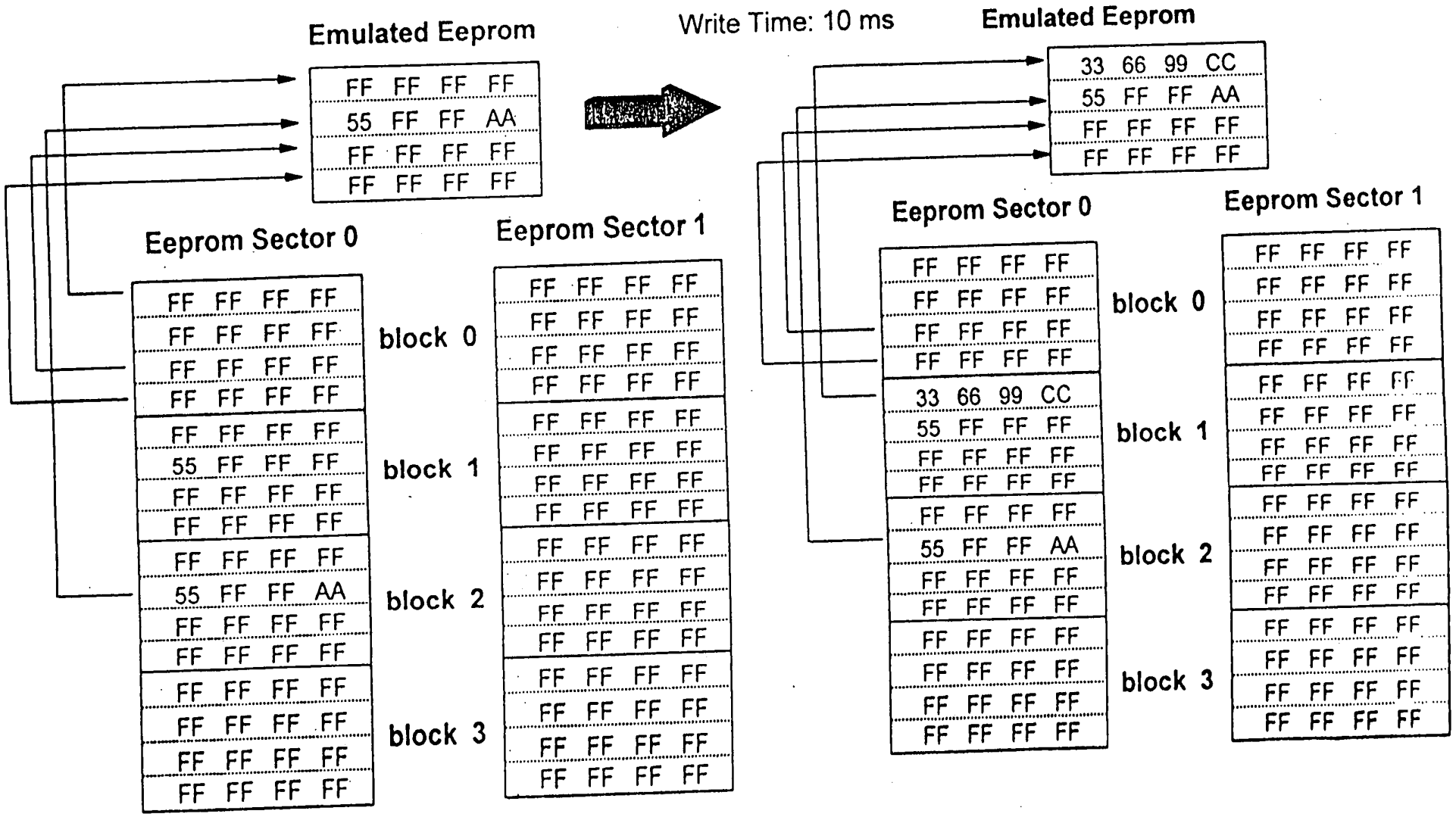

Emulated Eeprom
FF FF FF FF
55 FF FF AA
FF FF FF FF
FF FF FF FF
Write Time: 10 ms
Emulated Eeprom
33 66 99 CC
55 FF FF AA
FF FF FF FF
FF FF FF FF
Eeprom Sector 0
Eeprom Sector 1
block 0
block 1
block 2
block 3
Eeprom Sector 0
Eeprom Sector 1
block 0
block 1
block 2
block 3

FIG. 7

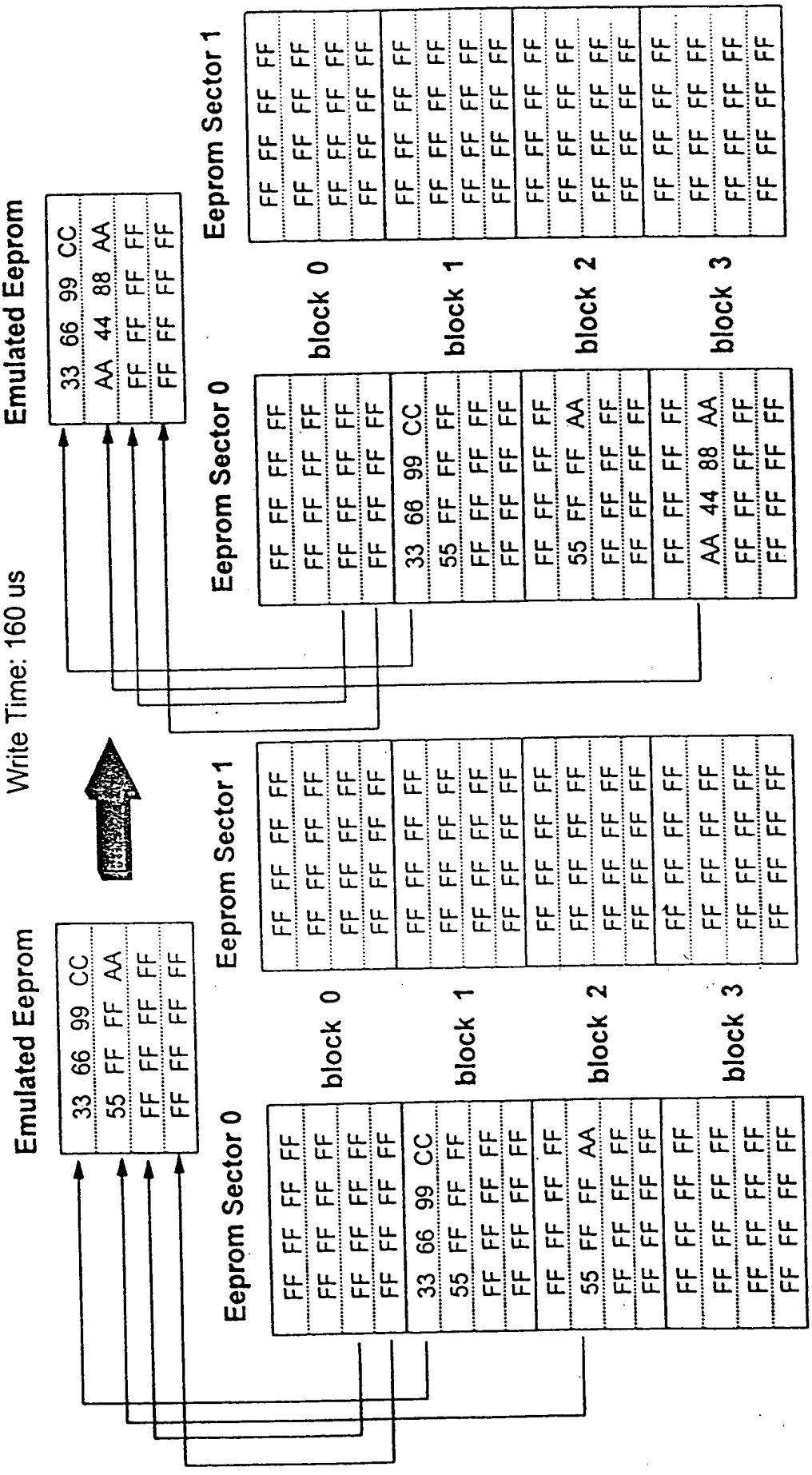

Emulated Eeprom
33 66 99 CC
55 FF FF AA
FF FF FF FF
FF FF FF FF
Write Time: 160 us
Eeprom Sector 0
Eeprom Sector 1
block 0
block 1
block 2
block 3
Emulated Eeprom
33 66 99 CC
AA 44 88 AA
FF FF FF FF
FF FF FF FF

FIG. 8

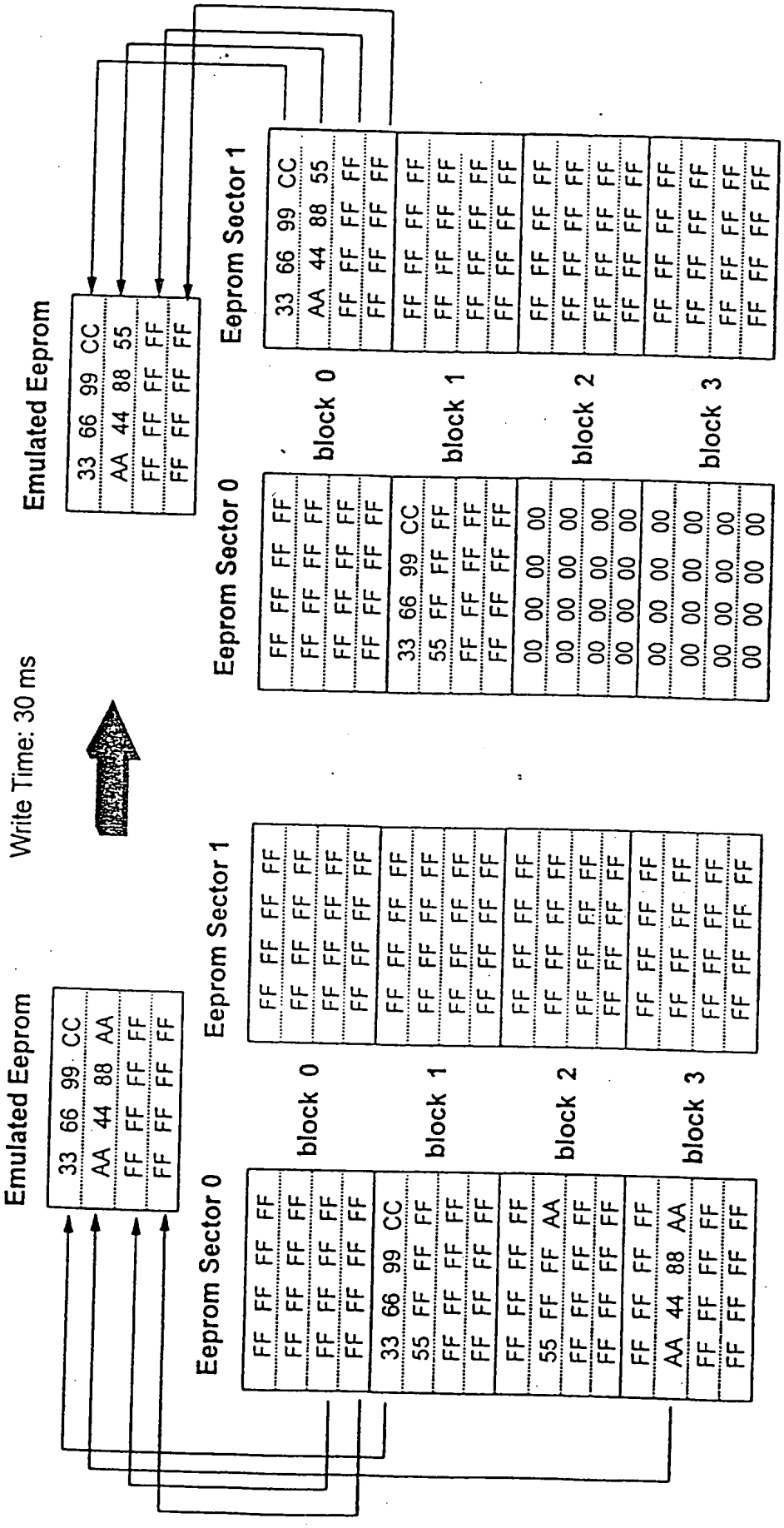

Emulated Eeprom
33 66 99 CC
AA 44 88 AA
FF FF FF FF
FF FF FF FF
Write Time: 30 ms
Eeprom Sector 0
Eeprom Sector 1
block 0
block 1
block 2
block 3
Emulated Eeprom
33 66 99 CC
AA 44 88 55
FF FF FF FF
FF FF FF FF
Eeprom Sector 0
Eeprom Sector 1
block 0
block 1
block 2
block 3

FIG. 9

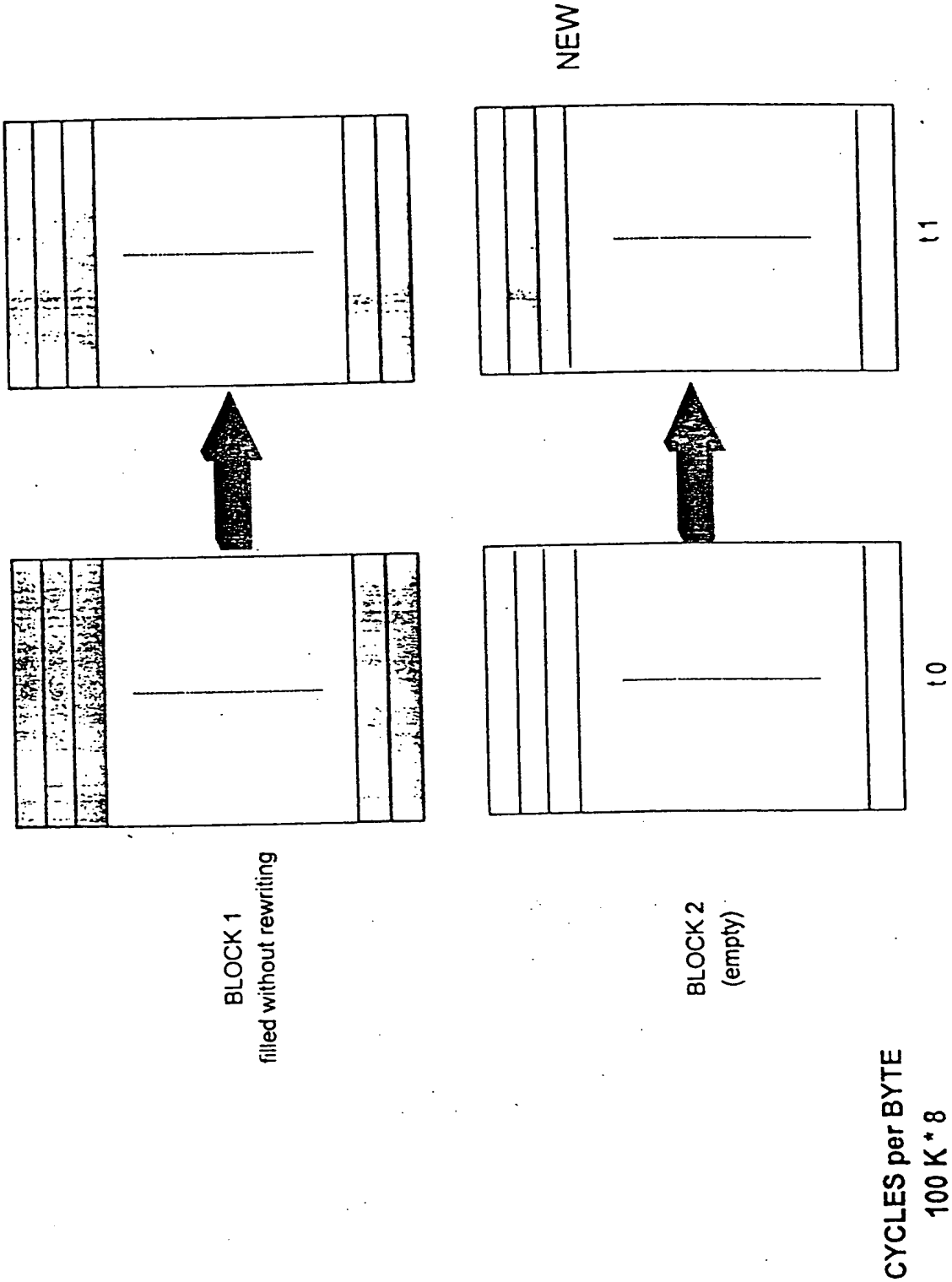

NEW
BLOCK 1
filled without rewriting
BLOCK 2
(empty)
t0
t1
CYCLES per BYTE
100 K * 8

FIG. 10

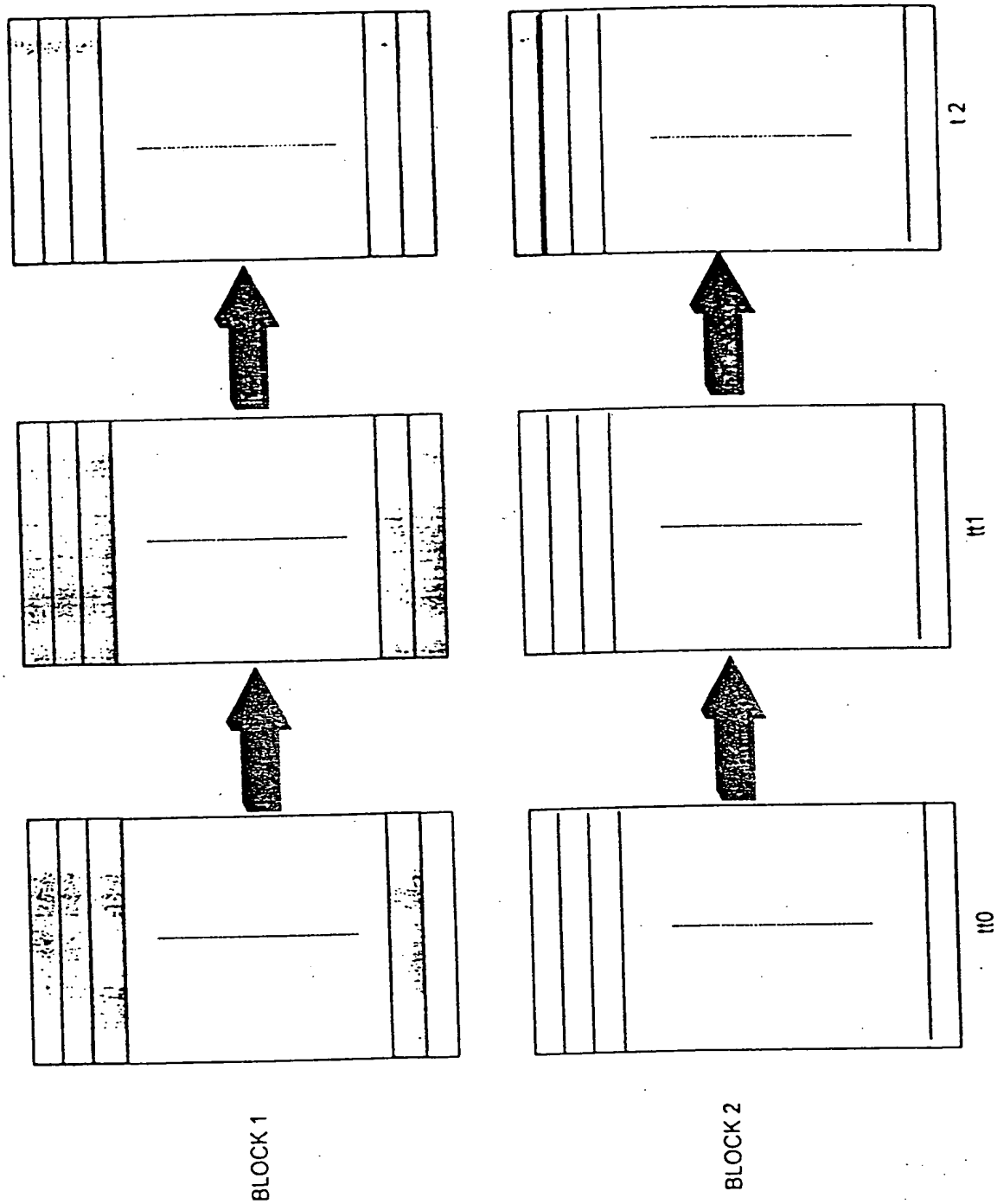


FIG. 11

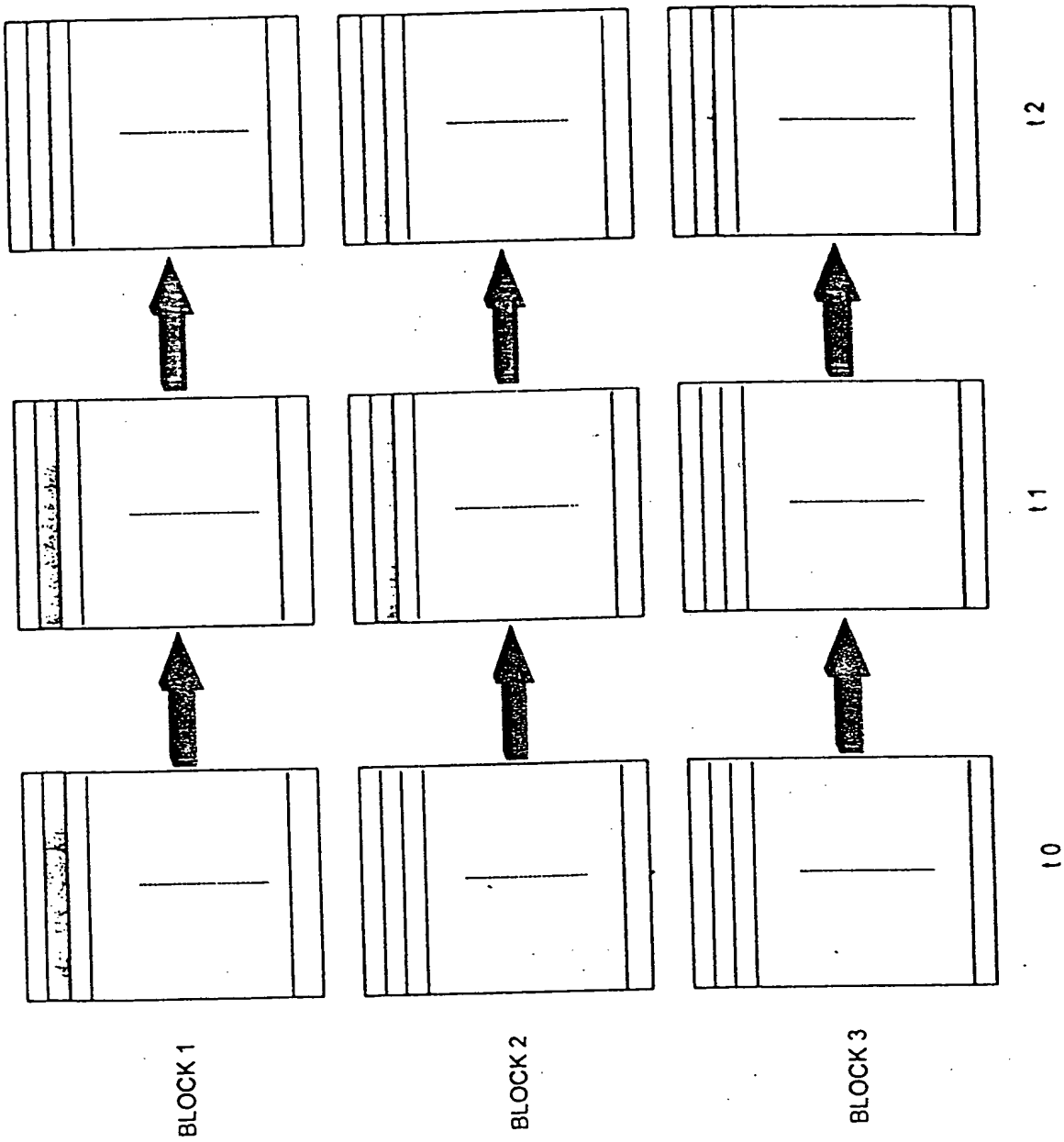
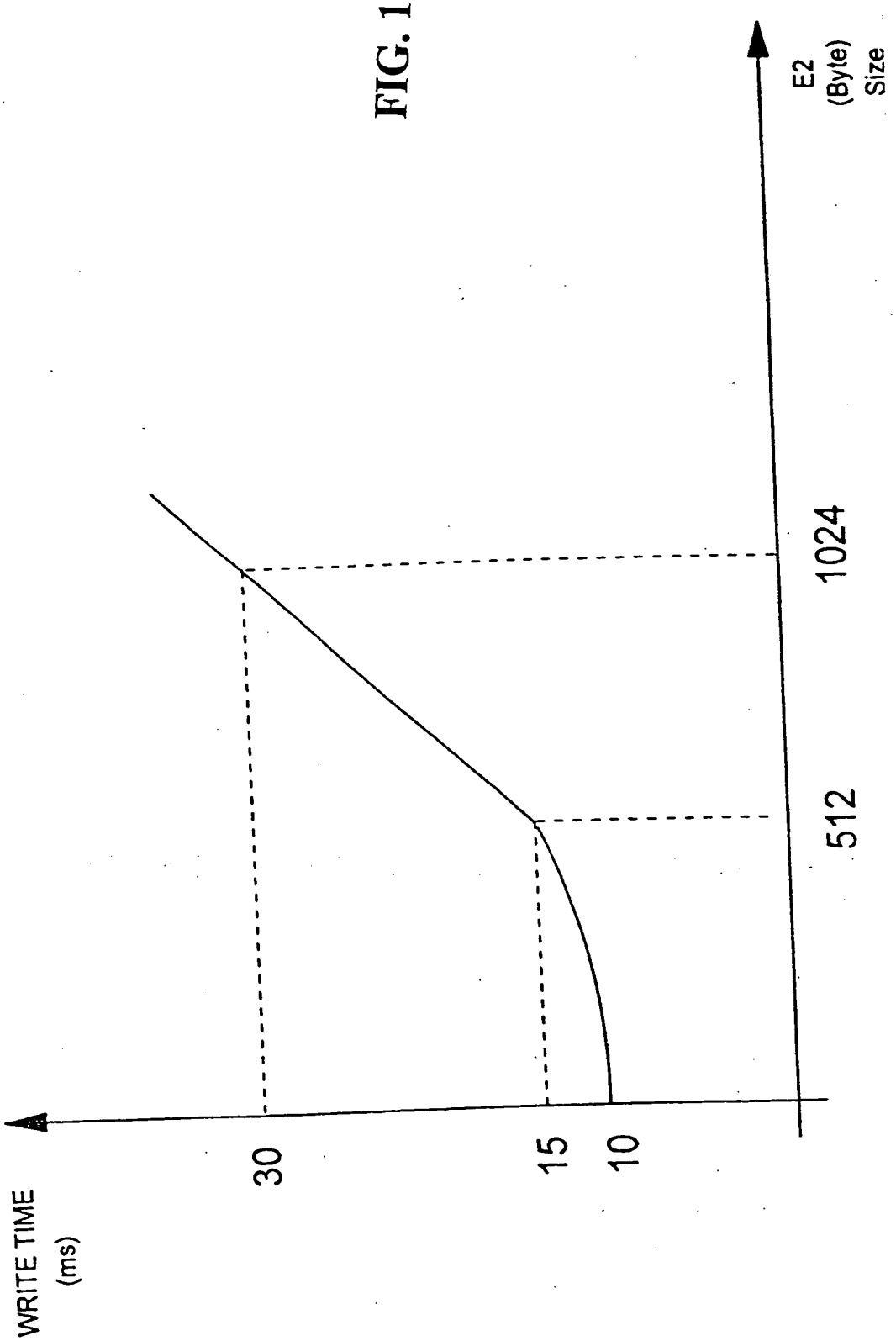


FIG. 12

FIG. 13



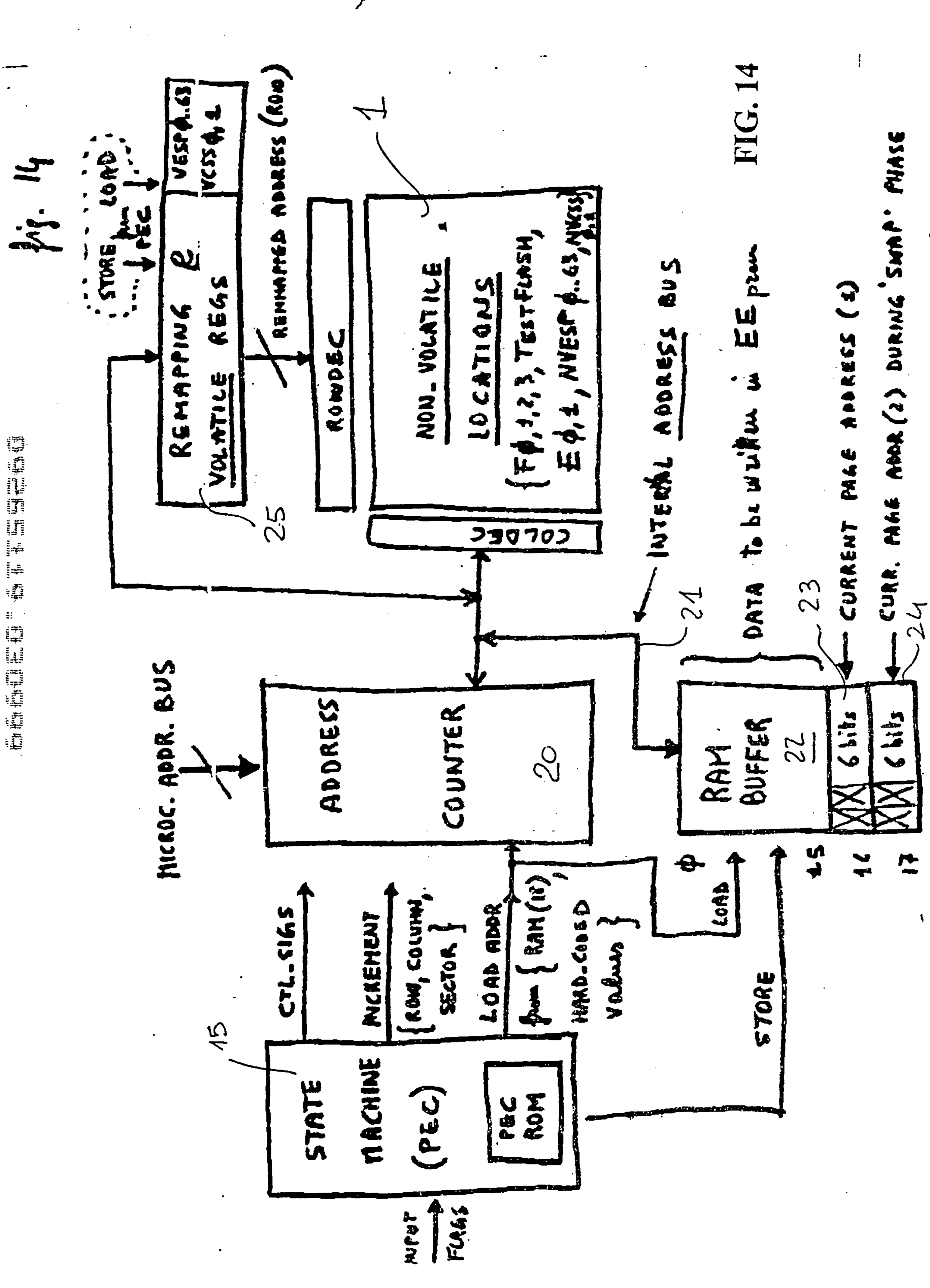


Fig. 14
STORE
LOAD
PEC
REMAPPING & VOLATILE REGS
VESPØ..63
VCSSØ,1
25
RENAMED ADDRESS (ROW)
ROWDEC
1
NON-VOLATILE LOCATIONS
{FØ,1,2,3, TESTFLASH, EØ,1, NVESPØ..63, NVCSSØ,1}
COLDEC
INTERNAL ADDRESS BUS
DATA to be written in EEprom
21
23
24
CURRENT PAGE ADDRESS (1)
CURR. PAGE ADDR (2) DURING 'SWAP' PHASE
RAM BUFFER
22
6 bits
6 bits
15
16
17
MICROC. ADDR. BUS
ADDRESS COUNTER
20
Φ
LOAD
STORE
CTL. SIGS
INCREMENT {ROW, COLUMN, SECTOR}
LOAD ADDR from {RAM (1/2), HARD-CODED values}
15
STATE MACHINE (PEC)
PEC ROM
INPUT FLAGS

FIG. 14